A. Amendments to the Specification:

Please replace the paragraph beginning at page 10, line 31, with the following amended paragraph:

External memory interface 203 provides an interface between the system bus 202 and the external main memory subsystem 103 (shown in FIG. 1). The external memory interface comprises a port to system bus 202 and a DRAM controller. An important feature of the present invention is that the memory accessed through external memory interface 203 is coherent as viewed from the system bus 202. All requests are processed sequentially on external memory interface 203 in the order of receipt of those requests by EMI unit 203. However the corresponding Store response packets may not be returned to the initiator on system bus 202 until the write operations are actually completed to DRAM. Since all the requests to the same address are processed in order (as they are received from the ~~SuperHyway~~ super highway interface) on the DRAM interface, the coherency of the memory is achieved.

Please replace the paragraph beginning at page 12, line 8, with the following amended paragraph:

FIG. 3 illustrates an exemplary transaction 300 comprising a request packet 301 and a response packet 303 for communication across ~~superhighway~~ super highway 202. Packets 301 and 303 comprise a unit of data transfer through the packet-router 305. Communication between modules 307 and 309 is achieved by the exchange of packets between those modules. Each module 307 and 309 is assigned or negotiates with packet router 305 for a unique address. In the particular example, each address is an unsigned integral value that corresponds to a location in the physical memory space of processor 201. Some of the address bits indicate the destination module and some of the address bits (called "offset

bits") indicate a particular location within that destination module. The size of the physical address, the number of destination bits, and the number of offset bits are implementation dependent selected to meet the needs of a particular implementation.